WHAT IS CLAIMED IS:

1. An address buffer used in a semiconductor device having N additive latency, where N is a natural number, the address buffer comprising:

(N/2) serially-connected flip-flops; and

an address control circuit which generates an address enable signal in response to a clock signal and a command signal;

wherein each of the (N/2) flip-flops is clocked to the address enable signal and sequentially latches an external address.

2. The address buffer of claim 1, wherein the address control circuit comprises:

an N-bit counter which responds to the clock signal;

an AND gate which receives output signals of the N-bit counter and performs an AND operation on the output signals of the N-bit counter; and

an OR gate which receives the command signal and an output signal of the AND gate, performs an OR operation on the command signal and the output signal of the AND gate, and outputs the address enable signal as an OR operation result.

3. The address buffer of claim 2, wherein the N-bit counter is reset in response to the command signal.

4. The address buffer of claim 1, wherein the command signal is activated in response to a data write command or a data read command.

5. An address buffer used in a semiconductor device having N additive latency, the address buffer comprising:

an N-bit counter which responds a clock signal;

an AND gate which receives output signals of the N-bit counter and performs an AND operation on the output signals of the N-bit counter;

an OR gate which receives the command signal and an output signal of the AND gate and performs an OR operation on the command signal and the output signal of the AND gate; and (N/2) serially-connected flip-flops;

wherein each of the (N/2) flip-flops is clocked to the output signal of the AND gate and latches and outputs an external address.

6. The address buffer of claim 5, wherein the N-bit counter is reset in response to the command signal.

7. The address buffer of claim 5, wherein the command signal is activated in response to a data write command or a data read command.

8. An address buffer used in a semiconductor device having N additive latency where N is a natural number, the address buffer comprising:

a shifting circuit including N/2 flip-flops;

an address control circuit which generates an address enable signal in response to a clock signal and a command signal;

wherein each of the (N/2) flip-flops is clocked to the address enable signal and sequentially latches an external address.

9. The address buffer of claim 8, wherein the address control circuit comprises:

an N-bit counter which responds to the clock signal;

an AND gate which receives output signals of the N-bit counter and performs an AND operation on the output signals of the N-bit counter; and

an OR gate which receives the command signal and an output signal of the AND gate, performs an OR operation on the command signal and the output signal of the AND gate, and outputs the address enable signal as an OR operation result.

10. The address buffer of claim 8, wherein the N-bit counter is reset in response to the command signal.

11. The address buffer of claim 8, wherein the command signal is activated in response to a data write command or a data read command.